IN THE CLAIMS

Claims 1-40 (Canceled)

41. (New) A semiconductor integrated circuit device, comprising:

a first potential point having a first potential;

a second potential point having a second potential;

a level-up level conversion circuit including:

first and second field-effect transistors of first conductivity type arranged to receive complementary input signals, wherein sources of the first and second field-effect transistors are coupled to the second potential point; and

third and fourth field-effect transistors of second conductivity type, wherein a source of the third field-effect transistor is coupled to the first potential point, a drain of the third field-effect transistor is coupled to a drain of the first field-effect transistor, a gate of the third field-effect transistor is coupled to a drain of the second field-effect transistor, a source of the fourth field-effect transistor is coupled to the first potential point, a drain of the fourth field-effect transistor is coupled to a drain of the second field-effect transistor and a gate of the fourth field-effect

transistor is coupled to a drain of the first field-effect transistor; and

a current source to limit a current flowing through the level-up level conversion circuit.

42. (New) The semiconductor integrated circuit according to claim 41,

wherein the level-up level conversion circuit further includes fifth and sixth field-effect transistors of second conductivity type arranged to receive the complementary input signals,

wherein a source of the fifth field-effect transistor is coupled to the drain of the third field-effect transistor, a drain of the fifth field-effect transistor is coupled to the drain of the first field-effect transistor, a source of the sixth field-effect transistor is coupled to the drain of the fourth field-effect transistor and a drain of the sixth field-effect transistor is coupled to a drain of the second field-effect transistor.

43. (New) The semiconductor integrated circuit device according to claim 41,

wherein the current source includes a seventh field-effect transistor of second conductivity type arranged to receive the second potential,

wherein a source of the seventh field-effect transistor is coupled to the first potential point and a drain of the seventh field-effect transistor is coupled to the sources of the third and fourth field-effect transistors.